

A REVIEW ON SILICON NANOWIRE: SHAPES, FABRICATION AND SCALING

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ABSTRACT

The needs of higher performance of electronic gadgets are progressively expected day in day out. In order to satisfy these needs and expectations, an exponential technology scaling had been done in metal oxide semiconductor field effect transistor MOSFET. The research investigated the scholars view in the field of silicon nanowire transistor (SiNWT) using qualitative approach in term of the method of fabrication, shape of the SiNWT, and scaling. The application of the SiNWT is also reviewed. In general, there are two major fabrication methods of Silicon Nanowire; Top-down approach and Bottom-up approach. Additionally, the shape of nanowire also plays a great role in the performance of the silicon nanowire. The shapes are circular rectangular, triangular, semi-cylindrical and cylindrical cross sections. A triangular shaped cross section SiNW FET having 300 nm channel length was designed and its short channel effects was described. For the fair comparison with previous works, the SCE parameters such as DIBL, ION/IOFF and SS were chosen. Moreover, due to tri-gate FET association with the corner effect which lead to high current leakage, which if not properly address would limit the potentials of the FET. In order to tackle the challenge, many effort has been made to minimize these effects, it is found that Rounding off the corner effect seem to be the best method to reduce the current leakage due to corner effect and enhanced device reliability. Semi-cylindrical silicon nanowire with both a short channel length of 65 nm and improved current leakage due to corner effect with slightly increase in DIBL is recommended among them. Moreover, the down scaling of silicon nanowire contributed a lot to the enhancement of the SiNW performance. Even though, further scaling to less than 7nm proof less effective, but Gate all around silicon nanowire promise a bright future for silicon nanowire Scaling.

Keywords: Drain Induce Barrier Lowering, Field Effect Transistor, Gate All Around , junctionless transistor, Short Channel Effects, Silicon nanowire.

1. INTRODUCTION

Semiconductor nanowires (NWs) have been widely studied as nanoscale building blocks for Nano electronics, since they can function as both devices and wires that access the devices. The uniqueness of physical properties of NWs and nanorods of metallic and semiconducting materials have drawn a lot of investigation [1]. NWs are synthesized from a range of different materials, such as Cadmium sulfide (CdS) and Zinc sulfide (ZnS), Gallium Nitride (GaN), p-GaN, Silicon (Si), germanium (Ge), or Indium phosphide (InP). They have been pull together as field-effect transistors (FETs), inverters, photodetectors, nanosensors, light-emitting diodes and lasers, decoder, nonvolatile memory and programmable logic. From an applications point of view, it has been shown that doped p type and n type SiNWS can be assembled to form p-n junctions, bipolar transistors, and complementary inverters. These results have led to the suggestion that SiNWs may become essential components for nanoscale electronics[1, 2]. very high mobility as a result of suppression of the ionize impurity, that are usually scattered at a very low temperature is considered a significant factor that nanowire and nanotubes are been the best candidate for high speed application [3]. There are many types of nanowire using different materials such as Germanium Nanowire, Silicon nanowire [4],

palladium nanowire [5] etc. the researcher is focus on Silicon nanowire due to attention it attracted as a promising future device. Silicon nanowire are used for in various field of endeavors such as biomedical sensors, biochemical sensors, optical components, fluid mechanics, Telecommunication, Electronics, power, *e. t. c.* due to its excellent sensitivity, low cost, and real time. When analytic molecules bind to a specific recognition molecule at the surface of the nanowire result to excellent sensitivity detection which is attached to their smaller size, and large surface to volume ratio, enabling local charge transfer which in turn change the current due to field effect [6]. Moreover, silicon nanowires were fabricated and produced using different approaches and methods such as bottom up and top down, the choice of synthesis approach depend on the aim and objective of the researcher. Some researchers focus on cross sections of silicon nanowire such as rectangular, circular, triangular [4], semi-cylindrical [7], cylindrical [8], electrical properties of nanowire, optical properties, width of nanowire. The aim of this research is to access scholarly view with regard to brief explanation of the design, fabrication, and application of silicon nanowire with view to gain knowledge for further studies especially in the field Electrical Engineering.

2. Materials and Methods

The method used in this report is literature review approach that is qualitative in nature, however the literature studied is further categorized under three (3) broad headings; Fabrication method of silicon nanowire, shapes, and length of the silicon nanowire. In addition, the knowledge gain from the study will serve as the foundation of recommendations for further studies. Moreover, some of the applications of silicon nanowire will be briefly highlighted. There are various methods and approaches were employed for different purpose, in this paper, some of the methods and approaches [9] will be briefly examine. In general, there are two major fabrication methods of Silicon Nanowire, top down and bottom up.

2.1 Cross Sectional Area of Silicon Nanowire

The needs of higher performance of electronic gadgets is progressively expected day in day out. In order to satisfy these needs and expectations, an exponential technology scaling had been done in metal oxide semiconductor field effect transistor MOSFET. However, task of making chip with large number of transistor is not an easy task. Major problems such as Short Channel Effects (SCE) occur as the result of miniaturization of the size of transistor. Due to scaling performance degradation occur, such DIBL, ION/IOFF ratio subthreshold slop (SS), quantum effect and velocity saturation. Till today, there are many different cross sections introduced in silicon nanowire FET design. There are two commonly used structures which are circular and rectangular cross sections. Currently triangular shaped silicon nanowire FET had attracted a fair amount of interest as well, due to its fabrication feature arises from anisotropic etch characteristics. A triangular shaped cross section Si NW FET having 300 nm channel length was designed and its short channel effects was described. For the fair comparison with previous works, the SCE parameters such as DIBL, ION/IOFF and SS were chosen[4]. Reference [7] also reported that, due to tri-gate FET association with the corner effect which lead to high current leakage, which if not properly address limit the potentials of the FET. In order to tackle the challenge, many effort has been made to minimize these effects, it is found that,

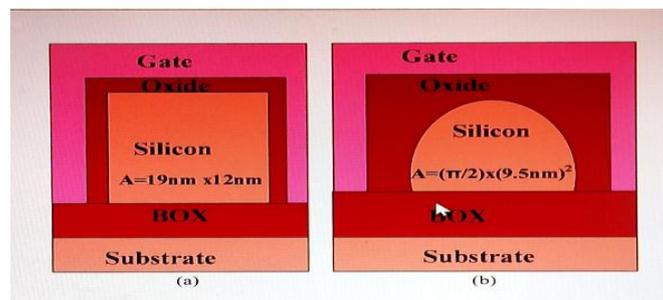


Figure 1. Structure of: (a) standard Triangle (b) Triangle semi-cylindrical channel

Rounding off the corner effect seem to be the best method to reduce the current leakage due to corner effect and enhanced device reliability. Therefore, semi-cylindrical channel was proposed

and analyzed using advance 3–D numerical simulator as shown in figure 1. It was found, based on simulation result, the leakage current has been reduced and is less sensitive to temperature effect. Moreover, cylindrical nanowire composed of silicon core and silica cladding having air hole in the core region has been characterized using FEM [8]. Moreover, hexagonal array of silicon nanowire as in figure 2, were also used by [10] , which according to them, have several advantages over square array as follows: first hexagonal array allow a tighter packing of vertical silicon nanowire (SiNW), for a given pitch between SiNWs. Secondly, it has dominant axes of 60 degrees, whereas square array has only two axes of 90 degrees apart.

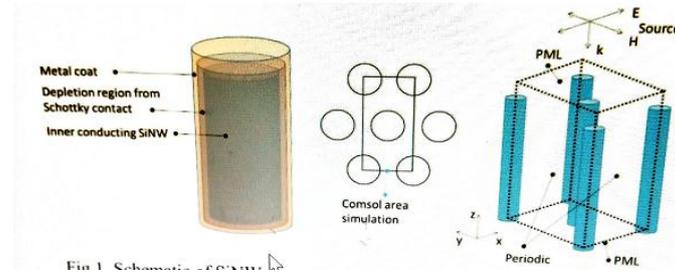


Figure 2. Schematic of SiNW in hexagonalarray used in COMSOL simulation

Third, it can be realize using naonsphere lithography to produce a high density SiNW in hexagonal array. Based on the cross section, observed above, the following table summarily compared their result. Table 2 summarize the findings of some of the researchers that focus on current leakage (I_{ON}/I_{OFF}), Drain Induce Barrier Lowering (DIBL), and subthreshold slope (SS), while Table 1 summarize the shape of the SiNW with their corresponding authors.

Table 1. Showing scholars who basically consider significantly the shape of the NWFET.

S/N	Tittle	Shape of NW	Ref.
1	Simulation of Trigate FET with Semi-Cylindrical Channel to reduce Corner Effect	Semi-circle	[7]
2	Triangular Shaped Silicon Nanowire FET Characterization using COMSOL Multiphysics	Triangular	[4]
3	Analysis of a Silica Cladded Silicon Nanowire Having a Deep Sub-Wavelength Central Air Hole	Cylindrical	[8]
4	Study of Optical Absorption in Hexagonal Silicon Nanowire Arrays with Radial Schottky Junction	Hexagonal	[10]

Table 2. Showing the results obtained by the schoolars.

Parameters	Rectangular	Triangular	Tri-gate FET Semi-cylindrical	cylindrical
Dimension	Channel length= 65nm	Height = 30nm Width = 30nm Channel length = 300nm	Channel length= 65nm	Diameter =50nm Channel length = 300nm
(I_{ON}/I_{OFF}) Ratio	93	1012	108	1012
DIBL (mV/V)	62	10.66	70	12.22
SS (mV/V)	70	56	88	60

2.2 Silicon Nanowire Scaling

The continuous miniaturization orscaling of silicon MOSFET, which characterized and proposed by Moore’s Law, is makes them smaller, faster, and cheaper. Over the past few decades, the success of modern microelectronics is based on miniaturization in silicon integrated circuits (IC’s), which has been well predicted by moor’s law that the number of transistors on a chip will double every 18 to 24 months.[11]. The scaling of SiNW is a best option for high performance improvement.

Many researchers in the field supported this claim. Not only [6] report an improvement of electrical characteristic using 10 μm long p-type poly-SiNW, which shows that a drastic change with drain bias polarity, the sub-threshold characteristics exhibit excellent behavior for both positive and negative drain bias application with a sub-threshold slope of 102.61 mV/decade. suggesting that poly silicon nanowire is good candidate for bio sensing operation with an achievable sensitivity around 800%, but also [12] said, there is high improvement achieved, of using 10 μm with the thickness of poly-SiNW gate is taken to 100 nm and 75 nm. A reasonable sub-threshold slope around 100 mV/dec for a feasible biosensor operation with doping concentration of $2 \times 10^{16}/\text{cm}^3$. The researcher further explained that, a widest range of doping concentrations can be chosen for 25 nm and 10 nm nanowire thicknesses with a maximum doping up to $10^{18}/\text{cm}^3$ while maintaining a promising sub-threshold slope around 95 mV/dec for a feasible biosensor design using polycrystalline silicon nanowires. Moreover, 300 nm length is investigated for the purpose of studying optical absorption of SiNW for high speed photodetector at 850 nm wavelength by [10], it was found the best lattice size at 800 nm. This unique design is a noble candidate for optical communication photodetector with a fast time of response, in which the radial Schottky junction provide fast photo generated carrier separations and the unique properties of SiNW which allows more light absorption due to wave guiding effect. Furthermore, due to some challenges such as short channel effect (SCE), Drain Induced Barrier lowering (DIBL), e.t.c, there is a shift of interest of researchers from ordinary SiNW scaling to Gate All Around SiNW Transistor (GAA SiNWT) as a future device, which have excellent immunity to SCE and outstanding transport performance[13, 14]. The device is described in the Figure 3.

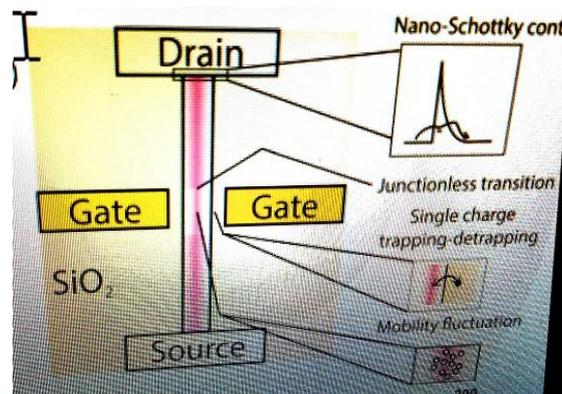


Figure 3. Gate All Around SiNW 1

The analog performance was analyzed in terms of transconductance, output conductance, voltage gain, early voltage and transconductance efficiency with gate length of 130 nm of GAA SiNW MOSFETs were fabricated on SOI wafers. The RF characterization showed relatively low cutoff frequency and maximum oscillation frequency [15], additionally, the GAA SiNWT provide better electrostatics aiming for exceptionally small device beyond 10 nm node. Because of high parasitic capacitances, Rf performance of Fin FETs is degraded. The electrostatic discharge (ESD) robustness of GAA SNWT is investigated from perspective of thermal analysis. The thermal conductance along the direction perpendicular to nanowire channel is found to be critical for heat dissipation in GAA SNWT. An optimized GAA SNWT structure is then proposed and fabricated. With the proposed devices, a record failure current density of $18.8\text{mA}/\mu\text{m}$ is achieved. The TLP test results are also consistent to the prediction of thermal analysis, which provides a new insight into the ESD optimization for future GAA SNWT technology[16,17,18]. [19] Also reported that, the further scale down to 2nm is GAA SiNW n-type FET was successfully fabricated and found Pelgrom coefficient of 7nm-wide nanowire FETs is much smaller than that of fully-depleted SOI FETs. Although, this research focus on silicon NW, a palladium based GAA NW is further proposed for the purpose Hydrogen gas sensing as illustrated in Figure 4.

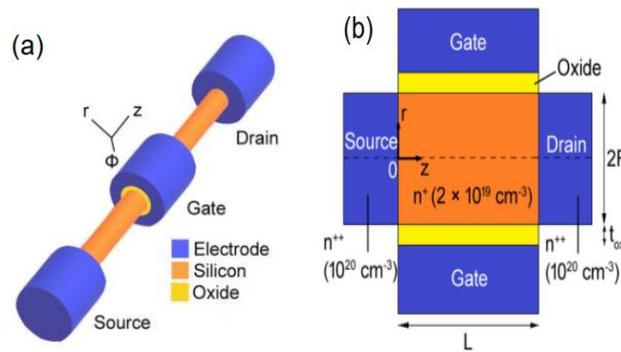


Figure 4. Palladium GAA NW (a) 3D and (b) 2D view[13]

There is a claim recently; MOSFETs with gate lengths below 4 nm performing very well apparently disregard the fundamental limit of source-to-drain direct tunneling (SDDT). Markov[20] investigated gate lengths between 8 and 3 nm, by simulating gate-all-around Si nanowire FETs with using the state-of-the-art atomistic quantum transport modeling as shown in Figure 5. It was found that at 3-nm gate length, the current is controlled by SDDT that leads to poor switching performance, which resulted from large source – drain leakage and even if the gate modulates the potential barrier between the source and drain appropriately well. However, at 6-nm gate-length, SDDT barely starts to degrade the subthreshold characteristics at large drain bias, and the ballistic ON-/OFF-current ratio is ~ 106 with a subthreshold swing of 70 mV/decade, on par with contemporary Si technology[20].

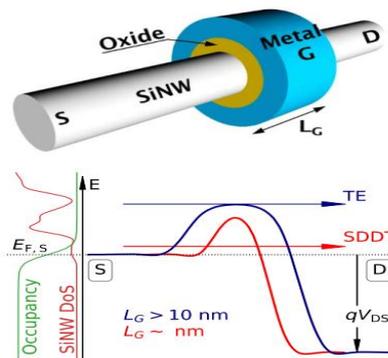


Figure 5. SiNW GAA (a) and Energy Band diagram in (b)[20]

2.3 Fabrication Method for Silicon Nanowire

There are varieties of different approaches in principle to fabricate silicon nanowires; these can be classified into bottom-up and top-down methods. The target application, strongly suggest the choice of fabrication method. From an application point of view, electron devices based on silicon nanowires are a natural addition of the downscaling of a silicon metal insulator semiconductor transistor. However, the unique properties also allow implementing new device concepts like the junctionless transistor and new functionalities like reconfigurability on the device level. Sensor devices may benefit from the high surface to volume ratio leading to a very high sensitivity of the device. In addition, solar cells and anodes in Li-ion batteries can be improved by exploiting the quasi one-dimensionality. In top-down fabrication, lithography is used to define the fabricated structure that is then transferred from the photo-resist to the substrate by etching or a related way of structuring. The already available material, to explore the advantage of scaling down device dimensions all the way to the 10 nm range by using photo lithography[21, 22, 23], [18] also use the top-down with dry-etching method. In the other hand, the bottom-up method, the material is added to the substrate in a self-organized manner. This techniques have the would-be used to construct very complex structures without the need of defining them in all details by a mask[21, 24].

3 APPLICATION OF SILICON NANOWIRE

Silicon nanowires have wide range of application in the field of engineering, Biomedical, Bio-Chemical application, internet of a thing, pressure sensors, photodetectors e.c.t.

3.1 Application of silicon nanowire in the field of Electrical Engineering.

Silicon nanowires find very wide application, in almost all the field of Engineering: such as Photovoltaic, Memory, Lithium Battery, Telecommunication, and internet of a thing, photodetectors, to mention but a few as depicted in Figure 6.



Figure 6. Some of the application of silicon nanowire in Electrical Engineering

a. Nanowire based photovoltaic

To obtain a high performance of nanowire based photovoltaic, there is a need to enhance the absorption spectra of semiconductor nanowires (NWs), understanding light trapping mechanisms is crucial. Light trapping mechanisms provide a design strategy to reach possible absorption enhancement. The optical response in NWs such as reflection, transmission, and absorption can be controlled by parameters like geometries, dimensions, arrangement, crystal phase, and dielectric function. Reducing the reflection either by aligning the SiNW arrays vertically or introducing porous structures to enhance the performance of photovoltaic [25, 26, 27, 28, 29]. Unselective near unity absorption necessary for high performance photovoltaic applications is conventionally achieved by $10(\text{DBRs})$ as the nger NWs or denser arrays of the NWs at the expense of increasing the material volume [27]. To reduce the cost, however, light trapping mechanisms in the NWs are the alternatives to enhance the absorption of the NW based on increasing optical path length of excited optical approaches in the NWs. Here, to achieve improved broadband absorption, we propose to enclose distributed Bragg reflectors substrate of the NWs [30, 31, 32]. Using the tapered NWs for the purpose of optical improvement due to antireflection enhancement with a graded-refractive-index (GRI) effect was observed. patterned co-integration of silicon nanowires (NWs) were applied for a novel photovoltaic (PV) Nano device [33, 34, 35, 36, 37, 38, 39, 40]. Coaxial nanowires can also be used to enhance photovoltaic [40]. Hexagonal and triangular III-Nitride nanowire (NW) photovoltaic devices.

b. Telecommunication

Recently, silicon-on-insulator (SOI) has become a good candidate for nonlinear photonics. Photons were firstly introduced to demonstrate the magical effects of quantum interference, which were produced by the spontaneous parametric conversion in the nonlinear crystal pumping with high power optical pulse source. The silicon waveguide has an ultrahigh nonlinear coefficient γ thanks to the high $\chi(3)$ of silicon and the strong light confinement. Due to the high refractive index contrast of SOI, the cross section of the silicon nanowire is just $0.1\mu\text{m}^2$ under single-mode condition. This, leading to large nonlinear parameter of nanoscale waveguide, which exhibit significant nonlinear effects with compact footprint using the nonlinear effects of spontaneous four-wave mixing (SFWM) within the silicon nanowire (SNW), broadband interrelated photon pairs are formed with continuous pumping light, which is beneficial for path entanglement [41].

c. Lithium battery

Portable electronic devices, electric vehicles and implantable medical devices needs a power that is rechargeable, because of this, there is great interest in developing rechargeable lithium batteries with higher energy capacity and longer life cycle for applications of this devices. because of the low discharge potential and the highest known theoretical charge capacity (4,200 mAh g) of silicon, it will serve as the best material for lithium batteries[30]. since they can overcome the pulverization and mechanical fracture during lithiation, silicon nanowires (SiNWs) have been useful as high-performance Li battery anodes[42]. Although [30] report that, more than ten times higher than obtainable graphite anodes, and much bigger than various nitride and oxide materials silicon anodes have limited applications, because silicon's volume changes by 400% upon lithiation, which results in pulverization and capacity fading. Here, we show that electrodes of silicon nanowire battery avoid these issues as they can accommodate large strain without pulverization, provide good electronic contact and conduction, and display short lithium insertion distances. We achieved the theoretical charge capacity for silicon anodes and maintained a discharge capacity close to 75% of this maximum, with little fading during cycling.

d. Memory technology

The SiNW biristor shows the outstanding memory characteristics such as a retention time of 10 s and a current sensing margin of $\sim 23\text{-}\mu\text{A}$ at room temperature. These memory characteristics originate from a positive feedback process resulting from impact ionization near the p-n junction. The nondestructive reading characteristics with a very high sensing margin show that the biristor can overcome the limited reading time of conventional 1T/1C DRAM. Furthermore, the two-terminal device structure enables a simple fabrication process and better reliability, which is free from oxide degradation by impact ionization[22]. [43] used complementary-metal-oxide-semiconductor-compatible top-down process technology fabricated vertical-Si-nanowire (SiNW) gate-all-around nonvolatile memory (NVM) devices of two different categories: junction based and junctionless (JL) by using Si nanocrystals (SiNCs) and silicon nitride (SiN) as trap layers. The improved performance and reduced process complexity of the devices are compared. The researcher, found that, the junction-based 50-nm vertical-SiNW memory device with a SiNC trap layer shows significant performance improvements on program/erase (P/E) speed and windows (3.5 V in 1-ms P/E at +15/-16 V) over a memory cell with a SiN trap layer (1.3 V in 1-ms P/E at +15/-16 V). On the other hand, the JL device with a SiN trap layer, realized on a highly scaled SiNW channel (down to 20 nm), is found to have comparable memory characteristics (3.2 V in 1-ms P/E at +15/-16 V) to a corresponding 20-nm SiNW junction-based cell (2.7 V in 1-ms P/E at +15/-16 V). Despite of that, the absence of junctions reduces process complexity and makes a vertical SiNW an appropriate platform for multilevel stacked ultrahigh density memory uses. Moreover, [44] suggest that Single electron charging effects in nanowires of silicon or polysilicon can be coupled to tunnelling barrier structures or conventional MOSFETs can be placed at the gate of the MOSFET to make memory cells. [45] report that, the NW cell exhibits faster program and erase (P/E) speed compared to the corresponding planar device with high-speed silicon-oxide-nitride-oxide-silicon (SONOS) nonvolatile memory cell in gate-all-around Si-nanowire (NW) architecture, was fabricated using a top-down method technology. It was further stated, increased electric field at the Si-SiO₂ interface, reduced effective tunnel barrier width, and low electric field in the blocking oxide; are the key contributors that leads to good data retention. Therefore, NW-based SONOS cell a prospective candidate for future high-speed low-voltage NAND-type nonvolatile Flash memory applications. [46]also report almost similar with addition of Nitrate silicon-oxide-nitride-nitride-oxide-silicon (SONNOS). There is possibility to use organic particles with silicon nanowire to produce further scaled device [47]. silicon nanowire MOSFETs is applied in memory[48].

e. Internet of a thing(IoT)

RF performance of silicon MOSFETs has been improved by the aggressive CMOS scaling. Especially the introduction of SOI technology offers great benefits of higher operating speed, less power consumption and higher design flexibility, which make it suitable for next generation IoT (Internet of a Thing) and 5G applications. Ultrathin body SOI can provide excellent electrostatic

control of channel, making it immune to SCE (short channel effect), but the fabrication of ultrathin body SOI is challenging. FinFETs have already revealed excellent gate control over SCE and gained great success in digital market. However, nanowire MOSFETs with GAA configuration offer even better electrostatics, targeting for extremely small devices beyond 10 nm node. RF performance of FinFETs is degraded because of high parasitic capacitance compared with their planar counterpart[15].

f. Application Of SiNW As Photodetector

We study a spectrometer consist of an array of silicon nanowire (Si NW) photodetectors, made above an array of planar photodetectors. This device would have manufacturing advantages, being based on Si technology and with all NWs defined in a single lithography step. The NWs would serve as photodetectors (converting incidence light to photocurrent) but would also filter the light transmitted onto the planar photodetectors. After the currents of photodetector is measured, the spectrum of light impacting on the device would be reconstructed mathematically[49].

3.2 Application of SiNW in the Biomedical

Personalized diagnosis system has become an important technical pillar toward the next generation healthcare system. Both microfluidic pumping and biomolecular detection are monolithically implemented by a 0.35 μ m standard CMOS technology, to harnessing momentums of CMOS technologies, it is exciting to integrate medical diagnostic technologies with personalized mobile platforms.[50] Among several biomolecular detection methods, silicon nanowire field-effect transistor (NWFET) sensors have been advanced for years. It is not only compatible to CMOS manufacturing technologies relate with other traditional bio-chemical and bio-sensors methods, but also realizes label-free and real-time detection[51–53]. Although previous works have successfully fabricated NWFET sensor devices. It is required to develop an interface circuit to transfer bio-signal into a diagnosis system[54]. It is also reported that, the biological element, inducing the single charge release models and procedures for the design of nanowires are propose and recommended[55]. SiNW-FETs and SiNW-ISFETs with enzymes measure protein, pH, potassium, sodium, ammonium, urea, creatinine, lactate, glutamate [57, 58, 59], DNA and event single virus particles due it's high sensitivity[59]. Silicon nanowire is also used to detect harmful gases[60, 61]. Further study shows that, Molybdenum disulfide/porous silicon nanowire (MoS₂/PSiNW) heterojunctions with different thicknesses as highly-responsive NO₂ gas sensors were obtained[62]. Nanoscale devices coordination for molecular communications, are good candidate for the purpose of encoding, transmitting, and receiving information. The attention given to the physical design of molecular receiver and transmitter is relatively low, envisioning biological synthetic cells with intrinsic molecular reception and transmission abilities as the future nanomachines. However, this assumption leads to a disagreement between the envisaged applications demanding complex communication interfaces and protocols, and the very limited computational capacities of the envisioned biological nanomachines[63]. The practicability of designing a molecular receiver, in a physical domain other than synthetic biology was examined, to meet the basic requirements of nanonetwork applications. It was first review the state-of-the-art biosensing methodologies to determine whether they can motivate a receiver design. It was revealed that, to design a molecular receiver, the nanoscale field effect transistor-based electrical biosensor technology (bioFET) is particularly a suitable starting point. With a conceptual approach, focusing on bioFET-based molecular receivers, it provides a guideline explaining on their operation principles, performance metrics, and design parameters. a simple model for signal flow in silicon nanowire FET-based molecular receiver its then provided [64].

3.3 Application of Nanowire As Pressure Sensor

Flexible pressure sensors are the cornerstone of electronic skins with tactile function. However, due to slow response speed and large hysteresis, which are caused mainly by the viscoelasticity and interfacial adhesion of flexible materials, flexible pressure sensors tend to have disadvantages. Silicon nanowires arrays is adopted to fabricate a pressure sensor with a piezo-capacitance when the Si nanowires are bending under pressure, which avoided the viscoelasticity and interfacial adhesion accompanying with common flexible materials. The sensor recorded unprecedented low hysteresis (~2.26%) and an extremely short response time (~3 ms). Large response

capacitance, ultralow detection limit (0.1 Pa), and good repeatability and stability, due to high sensitivity (up to ~8.2 kPa⁻¹), the sensor holds potential applications in advanced electronic skins, especially when high-precision and high-speed sensing are required[65]. It can also be used for sensing manifold air pressure and fuel pressure to decrease emission and fuel consumption; for measuring blood pressure[66].

4 RESULTS

4.1 Findings and Recommendations

The literature studied based on shapes of silicon nanowire is presented in the Table 3.

Table 3. Showing the result of silicon nanowire shapes based on dimension

Parameters	Rectangular	Triangular	Tri-gate FET Semi-cylindrical	Cylindrical
Dimension	Channel length= 65nm	Height = 30nm Width = 30nm Channel length = 300nm	Channel length= 65nm	Diameter =50nm Channel length = 300nm
(I_{ON}/I_{OFF}) Ratio	93	1012	108	1012
DIBL (mV/V)	62	10.66	70	12.22
SS (mV/V)	70	56	88	60

From the Table 3 above, the current I_{ON}/I_{OFF} ratio has increase from 93 in rectangular shape to 108 semi-cylindrical, to 1012 triangular and cylindrical, which shows that, the current leakage has been efficiently improved. This shows that the shape of the silicon nanowire has effect on the electrical characteristics. Among the four shapes, rectangular shows a high current leakage, followed by semi-cylindrical, the triangular and cylindrical show same least current leakage. The channel length of Triangular and Cylindrical shapes is almost five (5) times the channel length of the Rectangular and Semi-cylindrical. If the channel length decreases the DIBL increase. Therefore, semi-cylindrical silicon nanowire with both a short channel length of 65 nm and improved current leakage due to corner effect with slightly increase in DIBL is recommended among them. Even though, still there is need to look it the possibility to further reduce the DIBL without increasing the channel length. Hexagonal shape is developed in order to guide and reduces the optical losses of wavelength, which will enhance the performance in telecommunication industries. Based on the literature studies, the research shows, there are two major methods that are commonly used for silicon nanowire fabrication: Top-down fabrication approach has successfully enabled to scale down device dimensions all the way to the 10 nm range. Bottom-up approach have the potential to construct very complex structures without the need of defining them in all details. In terms of application, Silicon nanowires are used to fabricate devices such as NAND, inverter, NOR, memory *e.c.t.* it can also be used in telecommunication devices and industries, internet of a thing, power photovoltaic, photodetectors. In the field of biomedical, the silicon nanowire was not left behind, because, most of the recent biosensors such as DNA sensors, alpha thrombin, PH sensors *e.c.t.* are silicon nanowire based due to their reliability, speed, and size, which lead to less cost and power consumption. In chemistry, the ion sensors are build using silicon nanowire. Pressure sensors also used silicon nanowire. Therefore, silicon nanowire is a promising candidate for future technological advancement.

5 CONCLUSIONS

In conclusion, the shapes play a major role in reducing the current leakage in SiNW especially cylindrical shape. Even though, it has long channel length of 300 nm, followed by semi-cylindrical with 65 nm. The reduction of channel length is paramount in size and power consumption reduction. Therefore, semi-cylindrical silicon nanowire with both a short channel length of 65 nm and improved current leakage due to corner effect with slightly increase in DIBL is recommended among them. Even though, still there is need to look it the possibility to further reduce the DIBL without increasing the channel length. Hexagonal shape is developed in order to guide and reduces the optical losses of wavelength, which will enhance the performance in telecommunication industries.

Therefore, silicon nanowire is a promising candidate for future technological advancement. And further reduction of channel length below 65 nm is also recommended.

REFERENCES

- 1 Sarkar, J., Khan, G.G. and Basumallick, A. (2007). Applications and Synthesis via Porous Anodic. *Bulletin of Materials Science*, pages, vol. 30, no. 3, pp. 271-290.
- 2 Zheng, Y., Rivas, C., Lake, R., Boykin, T.B. and Klimeck, G. (2005). Electronic Properties of Silicon Nanowires. *IEEE Trans. Electron Devices*, vol. 52, no. 6, pp. 1097-1103.
- 3 Ahmadi, M.T., Saad, I., Ismail, R. and Arora, V.K. (2008). The Ultimate Drift Velocity in Two Dimensional Quantum Limit. *Second Asia Int. Conf. Model. Simul.*, pp. 980-984, 2008.
- 4 Yazeer, M.J., Za’Bah, N.F. and Alam, A.H.M.Z. (2016) Triangular Shaped Silicon Nanowire FET Characterization Using COMSOL Multiphysics. *Proceedings - 6th International Conference on Computer and Communication Engineering: Innovative Technologies to Serve Humanity, ICCCE 2016*, 2016, pp. 494-498.
- 5 Hu, Y. (2008) Single Palladium Nanowire: Synthesis via Electrophoresis Deposition and Hydrogen Sensing. *Electrical Engineering, University of Pittsburgh, Unpublished*, 23p.
- 6 Jan, M.I., Hakim, M.M.A., Shifat, T.A. and Nila, R. (2016). Bias Dependent Non-Linear Electrical Characteristics of Poly-Silicon Nanowire and Assessment of Biosensing Application Using Liquid Gate. *9th International Conference on Electrical and Computer Engineering*, pp. 206-209.
- 7 Hamid, F. and Ismail, R. (2013). Simulation of Trigate Fet With Semi-Cylindrical Channel To Reduce Effect. *UKSim 15th International Conference on Computer Modelling and Simulation*, pp. 712-716.
- 8 Rumman, N., Mesbah, M., Mahmud, T. and Alam, M.S. (2017). Analysis Of A Silica Cladded Silicon Nanowire Having A Deep Sub-Wavelength Central Air Hole. *Proc. 9th Int. Conf. Electr. Comput. Eng. ICECE 2016*, pp. 159-162.
- 9 Schmidt, V., Wittemann, J.V. and Go, U. (2010). Growth, Thermodynamics, and Electrical Properties of Silicon Nanowires. *2010 American Chemical Society*, pp. 361-388.
- 10 Surawijaya, A., Sulthoni, M.A. and Idris, I. (2017). Study of Optical Absorption in Hexagonal Silicon Nanowire Arrays with Radial Schottky Junction. *2017 Int. Symp. Electron. Smart Devices*, vol. 2, no. 1, pp. 260-263.
- 11 Ismail, R. (2015). Novel Device Architectures and Carbon Based Materials for Future Nanoelectronics. *2015 2nd International Conference on Information Technology, Computer, and Electrical Engineering (ICITACEE)*, pp. 1-1.
- 12 Haque, M.A., Hakim, M.M.A., Poly, L.P. and City, J.I. (2016). An Investigation of the Effects of Doping and Thickness on the Electrical Characteristics of Polycrystalline Silicon Nanowire Biosensors. *9th International Conference on Electrical and Computer Engineering 20-22 December, 2016, Dhaka, Bangladesh*, pp. 210-213.
- 13 Mokkalpati, S., Jaiswal, N., Gupta, M. and Kranti, A. (2019). Gate-All-Around Nanowire Junctionless Transistor based Hydrogen Gas Sensor. *IEEE Sens. J.*, vol. 1748, pp. 1-1.
- 14 Maneux, C., Pezard, J. and Larrieu, G. (2017). 1/F Noise In 3d Vertical Gate-All-Around Junction-Less Silicon Nanowire Transistors. *Eur. Solid-State Device Res. Conf.*, pp. 34-37.
- 15 Liu, L., Han, Q., Makovejev, S., Trelenkamp, S., Raskin, J.P., Mantl, S. and Zhao, Q.T. (2017). Analog and RF analysis of gate all around silicon nanowire MOSFETs. *Joint International EUROSOL Workshop and International Conference on Ultimate Integration on Silicon-ULIS, EUROSOL-ULIS 2017 - Proceedings*, 2017, pp. 176-179.

- 16 Li, M., Fan, J., Xu, X. and Huang, R. (2017). Investigation on Electrostatic Discharge Robustness of Gate-All-Around Silicon Nanowire Transistors Combined With Thermal Analysis. *IEEE ELECTRON DEVICE Lett.*, vol. 38, no. 12, pp. 1653-1656.
- 17 Prakash, O., Sharma, M. and Bulusu, A. (2016). Lateral Silicon Nanowire Based Standard Cell Design for Higher Performance. *2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, vol. 2, pp. 135-138.
- 18 Samya, T., Kobayashi, M., Sawamoto, N. and Hiramoto, T. (2017). Variability Characteristics of Gate-All-Around Polycrystalline Silicon Nanowire Transistors with 10nm-Scale Width. *2017, Materials Science, the Japan Society of Applied Physics*, pp. 33-34.
- 19 Hiramoto, T., Mizutani, T., Saraya, T., Takeuchi, K. and Kobayashi, M. (2016). Variability in Extremely Narrow (-2nm) Silicon Nanowire FETs Induced by Quantum Confinement Variation Due to Line Width Roughness, in *Solid-State and Integrated Circuit Technology (ICSICT), 13th IEEE International Conference*, pp. 4-6.
- 20 Markov, S., Kwok, Y., Li, J., Zhou, W., Zhou, Y. and Chen, G. (2019). Fundamental limit to scaling Si field-effect transistors due to source-to-drain direct tunneling. *IEEE Trans. Electron Devices*, vol. 66, no. 3, pp. 1167-1173.
- 21 Mikolajick, T. and Weber, W.M. (2015). Anisotropic Nanomaterials. *Anisotropic Nanomater*, pp. 1-26.
- 22 Lim, D., Kim, M., Kim, Y., Cho, J. and Kim, S. (2018). Nondestructive Readout Memory Characteristics of Silicon Nanowire Biristors. *IEEE Trans. ELECTRON DEVICES*, vol. 65, no. 4, pp. 1578-1582.
- 23 Alamo, J.A., Zhao, X., Lu, W. and Vardi, A. (2017). Towards Sub-10 nm Diameter InGaAs Vertical Nanowire MOSFETs and TFETs. *2017 Fifth Berkeley Symposium on Energy Efficient Electronic Systems & Steep Transistors Workshop (E3S), USA*, pp. 2-4.
- 24 Moeinian, A., Hibst, N., Geiger, D., Biskupek, J. and Strehle, S. (2017). Crystallinity of Silicon-Shells Deposited onto Germanium and Silicon Nanowires for Core-Shell Nanostructures and Nanotubes. *IEEE Trans. Nanotechnol.*, vol. 16, no. 5, pp. 736-740.
- 25 Najar, A., Al-jabr, A.A., Slimane, A.B., Alsunaidi, M.A., Ng, T.K. and Ooi, B.S. (2013). Effective antireflection properties of porous silicon nanowires for photovoltaic applications. *IEEE 2013 Saudi International Electronics, Communications and Photonics Conference*, pp. 8-11.
- 26 Parkash, V., Member, S. and Kulkarni, A.K. (2011). Optical Absorption Characteristics of Silicon Nanowires for Photovoltaic Applications. *IEEE Transactions on Nanotech*, vol. 10, no. 6, pp. 1293-1297.
- 27 Lin, C. and Povinelli, M. L. (2010). Optical Absorption Enhancement In Silicon Nanowire And Nanohole Arrays For Photovoltaic Application. *Conference on Lasers and Electro-Optics 2010*, pp. 1-2.
- 28 Routray, S.R. and Lenka, T.R. (2017). Spontaneous and Piezo-Phototronics Effect On Geometrical Shape Of Iii-Nitride Wurtzite Nanowires For High Ef Fi Ciency Photovoltaic Applications. *Micro Nano Lett.*, vol. 12, pp. 924-927.
- 29 Thalluri, S.M., Borme, J., Yu, K., Xu, J., Amorim, I., Gaspar, J., Qiao, L., Ferreira, P., Alpuim, P., and Liu, L. (2018). Conformal and continuous deposition of bifunctional cobalt phosphide layers on p-silicon nanowire arrays for improved solar hydrogen evolution. *2021 Springer Nature Switzerland AG. Part of Springer Nature*, vol. 11, no. 9, pp. 4823-4835.
- 30 Aghaeipour, M. and Pettersson, H. (2017). Enhanced Optical Absorption In Nanowires Over A Desire Range Of Wavelengths. *22nd Microoptics Conf. (MOC2017), Tokyo, Japan, Nov. 19 - 22, 2017*, no. 1, pp. 3-4.

- 31 Cui, L.F., Ruffo, R., Chan, C.K., Peng, H. and Cui, Y. (2009). Crystalline-Amorphous Core-Shell Silicon Nanowires for High Capacity and High Current Battery Electrodes. *Nano Lett.*, vol. 9, no. 1, pp. 491-495.
- 32 Jiang, X., Zhang, P., Zhang, J., Wang, J., Li, G., Fang, X., Yang, L. and Chen, X. (2018). High Performance of PEDOT: PSS/n-Si Solar Cells Based on Textured Surface with AgNWs Electrodes, *Nanoscale Res. Lett.*, vol. 13, no. 53. pp. 1-8.
- 33 Um, H. D. (2009). A Novel Photovoltaic Nanodevice Based On the Co-Integration of Silicon Micro and Nanowires Prepared By Electroless Etching with Conformal Plasma Doping. *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 551-554.
- 34 Huang, B.Y., Huang, B.Y., Liu, H. W., Chen, T.G., Chen, E.C., Chen, B.H., Liu, T.Y., Yu, P. and Meng, H. F. (2012). Solution-Processed Silicon Hybrid Heterojunction Photovoltaics with Silver Nanowires. *Conf. Rec. IEEE Photovolt. Spec. Conf.*, pp. 2537-2539.
- 35 Liu, Y., Blayney, G.J. and Guy, O.J. (2012). Rapid microwave growth of ZnO nanowires for low cost photovoltaics cells using reclaimed silicon substrates. *2012 IEEE Int. Conf. Electron Devices Solid State Circuit, EDSSC 2012*, pp. 1-3.
- 36 Chen, P. Cheng, K.Y., Pan, H.T., Yu, S.C., Weng, W.S., Lai, Y.C., Lin, Y.C., Chen, Y.C., Li, M.C., Hu, H. W., Yu, P. and Meng, H.F. (2014). Projected Efficiency of Organic / Inorganic Hybrid Tandem Solar Cells. *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)*, pp. 2-4.
- 37 Zhou, H., Lentaris G., Hiralal, P., Butler, T., Unalan, E., Amaratunga G. and Colli, A. (2012). Photovoltaic measurements in carbon nanotube - amorphous silicon core/shell nanowire. *2012 38th IEEE Photovolt. Spec. Conf.*, pp. 1944-1947.
- 38 Nakamura, H. (2011). High-Efficiency Si-Nanowire Photovoltaic Devices with Optimal Tip Head Design. *2011 11th IEEE International Conference on Nanotechnology*, pp. 2-5.
- 39 Road, M. and City, J.I. (2017). Feasibility of Silicon Nanowire's Electrical Characteristics Modulation Using Substrate Bias for Tunable Biosensor Design. *2017 IEEE Region 10 Humanitarian Technology Conference (R10-HTC)*, pp. 21-23.
- 40 Wang, B., Leu, P., Wang, B. and Leu, P.W. (2012). Tunable and selective resonant absorption in vertical NWs Tunable and selective resonant absorption in vertical nanowires. *Optics Letters*, vol. 37, Issue 18, pp. 3756-3758.
- 41 Kurniawan, O. and Li, E.P. (2009). Study of a Single Coaxial Silicon Nanowire for On-Chip Integrated Photovoltaic Application. *IEEE Proceedings of the 2009 12th International Symposium on Integrated Circuits*, pp. 314-317.
- 42 Shao, J., Yu, Y. and Wang, Y. (2012). Quantum interference of the non-degenerate photon pairs in silicon nanowire. *2017 Conference on Lasers and Electro-Optics Pacific Rim (Optical Society of America, 2017)*, no. 2012, pp. 2-4.
- 43 Klankowski, B.A., Pandey, G.P., Cruden, S.A., Ma, Y., Liu, D., Zhang, W., Wang, H. and Li, J. (2014) High-Rate Lithium-ion Battery Anodes Based on Silicon-Coated Vertically Aligned Carbon Nanofibers. *Proceedings of the 14th IEEE International Conference on Nanotechnology Toronto, Canada, 2014*, pp. 22-23.
- 44 Seo, K., Wober, M., Steinvurze, P., Schonbrun, E., Dan, Y., Ellenbogen, Tal. and Crozier, K.B. (2011). Multicolored Vertical Silicon Nanowires, pp. 1851-1856.
- 45 Ahmed, H. (1999). Single Electron and Few Electron Memory Cells. International Electron Devices Meeting (IEDM) 1999. Technical Digest (Cat. No.99CH36318), pp. 363-366.
- 46 Fu, J., Singh, N., Buddharaju, K.D., Teo, S.H.G., Shen, C., Jiang, Y., Zhu, C.X., Yu, M.B., Lo, G.Q. and Balasubramanian N. (2008). Si-nanowire based gate-all-around nonvolatile SONOS memory cell," *IEEE Electron Device Lett.*, vol. 29, no. 5, pp. 518-521.

- 47 Lin, Y.R., Chiang, Y.W., Lin, Y.H., Wang, W.C. and Wu, Y.C. (2018). Comparison with Nitride Interface Defects and Nanocrystals for Charge Trapping Layer Nanowire Gate-All-Around Nonvolatile Memory Performance. *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 493-498.
- 48 Tsai, C.Y., Chen, P., Huang, Y.Y., Pan, H.T., Yu, P. and Meng, H.F. (2013). 11 % - Efficiency Hybrid Organic/Silicon-Nanowire Heterojunction Solar Cell with an Intermediate 1, 1-bis [(di-4-tolylamino) phenyl] cyclohexane Layer. *39th IEEE PVSC*, no. 1, pp. 4-6.
- 49 Park, O. (2008). Silicon Nanowire CMOSFETs: Fabrication, Characteristics, and Memory Application. *2008 9th International Conference on Solid-State and Integrated-Circuit Technology*, pp. 2-5.
50. Meng, J., Li, S. and Crozier, K.B. (2017). Wavelength-Multiplexed Spectrometer Based on Silicon Nanowire Photodetector Array. *The European Conference on Lasers and Electro-Optics 2017, Munich Germany, 25–29 June 2017*, vol. 523, no. 4, pp. 36-67.
- 51 Liu, T.Y., Wang, I.S., Yen, P.W., Lin, S.C., Lin, K.C., Jheng, J.S., Chang, D.Y. and Lin, C.T. (2017) CMOS-based biomolecular diagnosis platform. *2017 IEEE 12th International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*. pp. 96-100.
- 52 Cai, Q (2016). State Key Laboratory of Transducer Technology, Shanghai Institute of Microsystem and Information of Functional Materials. Shanghai Institute of Microsystem and School of Electronic Engineering, Bangor University, B,” *MEMS 2016, Shanghai, CHINA, 24-28 January 2016*, vol. 25, no. January, pp. 294-297.
- 53 Ahn, J.H., Kim, J.Y., Choi, K., Moon, D., Kim, C.H., Seol, M.L., Park, T.J., Yu, S. and Choi, Y.K. (2012). Nanowire FET biosensors on a bulk silicon substrate. *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2243-2249.
- 54 Hurtado, A., Jevtics, D., Guilhabert, B., Gao, Q., Tan, H.H. and Dawson, M.D. (2017). Transfer printing of semiconductor nanowire lasers. *Journals & magazines IET Optoelectronics*, vol. 12, Issue 1, pp. 30-35.
- 55 Shen, S.H., Ting, C.Y., Liu, C.Y., Cheng, H., Liu, S.I. and Lin, C.T. (2014). A Silicon Nanowire-Based Bio-Sensing System with Digitized Outputs for Acute Myocardial Infraction Diagnosis. *2014 IEEE-EMBS Int. Conf. Biomed. Heal. Informatics, BHI 2014*, pp. 660-663.
- 56 Carmignani, C., Rozeau, O., Scheiblin, P. and Vinet, M. (2016). Fine charge sensing using a silicon nanowire for biodetection. *2016 Int. Symp. VLSI Technol. Syst. Appl. VLSI-TSA 2016*, pp. 9-10.
- 57 Adhyaksa, G.W.P., Johlin, E. and Garnett, E.C. (2017). Nanoscale Back Contact Perovskite Solar Cell Design for Improved Tandem Efficiency. *Nano Lett.*, vol. 17, no. 9, pp. 5206-5212.
58. Lale, A., Grappin, A., Bourrier, D., Mazenq, L., Lecestre, A., Launay, J. and Temple-Boyer, P. (2017). Design, Realization And Characterization Of All-Around SiO₂ / Al₂O₃ Gate, Suspended Silicon Nanowire Chemical Field Effect Transistors Laas-Cnrs, Université De Toulouse, F-31400 Toulouse, France Device Fabrication. *IEEE*, vol. 978, no. 1, pp. 1508-1511.
59. Lee, I., Lee, S. W., Lee, K.Y., Park, C., Kim, D., Lee, J.S., Yi, H. and Kim, B. (2016). A Reconfigurable and Portable Highly Sensitive Biosensor Platform for ISFET and Enzyme-Based Sensors. *IEEE Sens. J.*, vol. 16, no. 11, pp. 4443-4451.
60. Gong, X., Zhao R., and Yu, X. (2018). A 3-D-Silicon Nanowire FET Biosensor Based on a Novel Hybrid Process. *Jour. Microelectromechanical Syst.*, vol. 99, pp. 1-7.
61. Gao, A., Wang, Y., Yang, X., Wang, Y. and Li, T. (2017). Ultrasensitive Bioelectronic Nose Based On CMOS- Compatible Silicon Nanowire Array. *IEEE Trans.*, no. 111, pp. 7-9.

62. Chang, Y., Qu, H., Duan, X., Mu, L. and Reed, M.A. (2016). VOC Detection Using Multimode E-nose Composed of Bulk Acoustic Wave Resonator and Silicon Nanowire Field Effect Transistor Array, vol. 1, pp. 5-7.
63. Zhao, S., Li, Z., Wang, G., Liao, J., Lv, S. and Zhu, Z. (2018). Highly Enhanced Response of MoS₂/Porous Silicon Nanowire Heterojunctions to NO₂ at Room Temperature. *RSC Adv.* vol. 8, no. 20, pp. 11070-11077.
64. Kuscu, M. and Akan, O. B. (2016). On the Physical Design of Receiver for Molecular Communications. *IEEE Sensors Journal*, vol. 16, no. 8, pp. 2228-2243.
65. Kuscu, M. and Akan, O.B. (2016). Modeling and Analysis of SiNW FET-Based. *IEEE Trans. Commun.*, vol. 64, no. 9, pp. 3708-3721.
66. Cheng, W., Yu, L., Kong, D., Yu, Z., Wang, H., Ma, Z., Wang, Y. and Wang, J. (2018). Fast-response and Low-hysteresis Flexible Pressure Sensor Based on Silicon Nanowires. *IEEE Electron*, vol. 3106, pp. 1-4.
67. Lee, Y.C., Parviz, B.A., Chiou, J.A. and Chen, S. (2003). Packaging for Microelectromechanical and Nanoelectromechanical Systems. *Journals & Magazines IEEE Transactions*, vol. 26, no. 3, pp. 217-226.